IFW AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT	:	Cornelis Bernardus Aloysius Wouters		
SERIAL NO.	:	09/846,596	EXAMINER	: Woo H. Choi
FILED	:	April 30, 2001	ART UNIT	: 2186
FOR	:	METHOD, SYSTEM, AND COMPUTER PROGRAM		

APPEAL BRIEF TRANSMITTAL LETTER

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA. 22313-1450

Dear Sir:

Appellants respectfully submit three copies of a Brief For Appellants that includes an Appendix with the pending claims. The Appeal Brief is now due on December 7, 2004.

Appellants enclose a check in the amount of $340.00 covering the requisite Government Fee.

Should the Examiner deem that there are any issues which may be best resolved by telephone communication, kindly telephone Applicants undersigned representative at the number listed below.

Respectfully submitted,
Russell Gross
Registration No. 40,007

By: Steve Cha
Attorney for Applicant
Registration No. 44,069

Date: December 7, 2004

Mail all correspondence to:
Russell Gross, Registration No. 40,007
US PHILIPS CORPORATION
P.O. Box 3001
Briarcliff Manor, NY 10510-8001
Phone: (914) 333-9608
Fax: (914) 332-0615

Certificate of Mailing Under 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to MAIL STOP APPEAL BRIEF-PATENTS, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA. 22313 on **December 7, 2004**.

Steve Cha, Reg. No. 44,069
(Name of Registered Rep.)

(Signature and Date)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	**Cornelis Bernardus Aloysius Souters**
Application No.	:	**09/846,596**
Filed	:	**April 30, 2001**
For	:	**METHOD, SYSTEM, AND COMPUTER PROGRAM**

APPEAL BRIEF

On Appeal from Group Art Unit 2186

Date: December 7, 2004

Russell Gross
Registration No. 40,007
By: Steve Cha
Attorney for Applicant
Registration No. 44,069

CERTIFICATE OF MAILING UNDER 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450 Alexandria, Va 22313-1450 on December 7, 2004.

Steve Cha, Reg. No. 44,069
(Name of Registered Representative)

(Signature)

TABLE OF CONTENTS

TABLE OF CASES

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the present application, U.S. Philips Corporation, and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-3, 5-9 and 11-17 have been presented for examination. All of these claims are pending, stand finally rejected, and form the subject matter of the present appeal.

IV. STATUS OF AMENDMENTS

The Amendment after Final Office Action filed August 11, 2004 has been entered.

V. SUMMARY OF THE INVENTION

The invention is related to the field of semiconductor memory and more specifically to a method for managing the storage utilization to provide substantial uniform erasing/writing of data into memory blocks and prevent one block of the memory from being erased/written into more often than others. In one aspect to the invention, the memory blocks of the memory have an associated counter for keeping track of the number of times a

mutation (erasure) of a block has been carried out. A control unit is able to determine the number of mutations of a block by reviewing the counter. When the value of the counter associated with a block is less than a limit value, the control unit erases the block and increments the associated counter. When the value of the counter associated with a block is substantially equal to the limit value, then a second block is accessed. When a majority of the counters of all the blocks exceed the limit value or have reached it, the limit value can be raised. The increasing of the limit value allows blocks whose counter value had reached the limit value are now again eligible for being erased.

VI. ISSUE

The issues before this board are whether:

1. claims 1-3, 5-9, 11-13 and 15-17 are unpatentable under 35 USC §103(a) over Assar (WO95/10083) or in view of the combination of Assar and Bruce (USP No. 6,000,006);

2. claim 14 is unpatentable under 35 USC §103(a) over Assar and Bruce and further in view of Marsters (USP No. 6,092,160);

3. claims 15 and 17 are unpatentable under 35 USC §112, first and second paragraphs as failing to comply with the written description and for failing to particularly point out the subject matter claimed.

VII. GROUPING OF THE CLAIMS

With regard to Issues 1 and 2, claims 1-9, 11-13 and 15-17 stand or fall together.

With regard to Issue 3, claims 15 and 17 stand or fall together.

VIII. ARGUMENT

I. Rejection Under 35 USC §103(a) in view of Assar

Claims 1-3, 5-9, 11-13 and 15-17, stand rejected under 35 USC §103(a) as being obvious in view of Assar (WO95/10083). The examiner contends that Assar discloses a method of data management system containing the elements recited in claim 1. However, "Assar does not specifically disclose that the limit value is increased when a predetermined number ... of the blocks ... exceed the limit value." (See p. 4, first full paragraph, Final Office Action, July 7, 2004). The examiner further contends that "[o]n the other hand Assar discloses a functionally equivalent method where the limit value is effectively increased when a predetermined number ... of the blocks ... reach a maximum value by resetting the counters." Id.

Difference Between the Claimed Invention and the Primary Reference – Assar

The present invention, as recited, for example in claim 1, is a method for managing the distribution of the number of times a mutation (erasure) of a cell block occurs by allowing erasures up to a predetermined limit and limiting further erasures of a cell block that achieves the limit until a substantial number of other cells have been erased substantially the same number of times. A total count of the number of erases is maintained for each cell and the predetermined limit value is increased when a majority of cell blocks has achieved the predetermined number of erasures. This allows further erasures of cell blocks that were previously inhibited from being erased.

Assar teaches a method for managing the distribution of the number of times an erasure of cell block may occur by allowing erasures up to a predetermined limit and inhibiting further erasures of a cell block that has achieved the limit. When a substantial

number of cell blocks have achieved the predetermined limit, the counters associated with each cell block is erased in an erase cycle. The erased counters allow the cell blocks to again be erased.

The examiner, in the Final Office Action, distinguishes the present invention, as recited in the independent claims, e.g., claim 1, and the teachings of Assar, as "there's [sic] a need to keep track of the total number of erase cycles ... to determine the remaining life of a device. One would be motivated to ... [use] the method of increasing the limit value while keeping the total counts intact to be able to keep accurate track of the total number of erase cycles. On the other hand, ... keeping the limit value while resetting the counter has the advantage of having smaller counters. However, since the total erase count is reset, the system can easily track the overall wear level by keeping track of the number of wear-level cycle operation." (see p.5, second paragraph).

In support of the rejection of the claims the examiner states that "A flash memory system designer would be motivated to choose one or the other depending on his/her preference and design criteria." Id.

No Motivation Exists for the Examiner's Proposed Modification of Assar

Contrary to what the examiner states, there is neither motivation to develop the features of the present invention nor that the features of the present invention are merely a design criteria. Assar teaches a method for managing the number of erase cycles that may be performed on a selected memory block by maintaining a number of flags and counters. For example, for each memory block Assar teaches an eight bit wear out leveling counter, a one-bit erase inhibit flag, a one-bit used flag and a one-bit old flag. Assar teaches that the leveling counter is increased for each erase of a corresponding block and "[o]nce the wear

out leveling count ... reaches a predetermined maximum value, the erase inhibit flag for that information block is set. (See Assar, p. 20, lines 19-22). Data is then shifted to data blocks that have the lowest wear out leveling counts until the predetermined maximum is achieved and the erase inhibit flag is set. Id., lines 24-35). "Periodically all ... storage pairs, [data block and corresponding information block] will have maximum wear out leveling count values and set erase inhibit flags. At such time, a clean-out erase cycle is performed. During a clean-out erase cycle the wearout leveling count and the erase inhibit flag are erased for all information blocks." Id., p. 20, line 36 –p. 21, line 5.

Accordingly, Assar teaches erasing memory blocks up to a maximum limit and then erasing this accumulated information during an erase cycle. Assar fails to teach or suggest maintaining a count of the number of erase cycles, to obtain a total number of erasures, as the examiner has suggested.

The law is clear that there must be some teaching in the reference to support their use in the particular claimed combination. See Smithkline Diagnostics, Inc., v. Helena Labs Corp., 859 f.2d 878, 887, 8 USPQ 2d 1468, 1475 (Fed. Cir. (1988). Nothing in Assar teaches or suggests maintaining a total count of the number of erasures of each memory block or increasing the maximum number of allowable erasures when a majority of blocks have a count at the maximum count, as is recited in the claims.

In the matter of obviousness, the court has found that:

> "an examiner ... may often find every element of a claimed invention in the prior art. If identification of each claimed element of the prior art was sufficient to negate patentability, very few patents would ever issue. Furthermore rejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner ... to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention ... To counter this potential weakness in the obviousness construct, the suggestion to combine

> requirements stands as a critical safeguard against hindsight analysis and rote application of the legal test for Inc. 231 F. 3d. 1339, 56 USPQ2d. 1641, 1644 (Fed. Cir. 2000). quoting In re Roobviousness. Yamanouchi Pharmaceutical Co. v. Danbury Pharmacal, uffet, 149 F.3d 1350, 1357-58, 47 USPQ 2d 1453, 1457 (Fed. Cir. 1998)"

In this case, the examiner's proposed modification of Assar is not merely a design criteria but is an impermissible use of the present invention as a blueprint to develop an erase cycle counter feature and additional complexity that Assar fails to teach or suggest.

In view of the above, applicant submits that claims 1-9, 11-13 and 15-17 are patentable over the teachings of Assar.

Examiner's Proposed Modification of Assar Fails to Arrive at the Present Invention

To establish a prima facie case of obviousness of a claimed invention, all the claim limitations must be taught or suggested in the prior art. See *In re* Royka, 490 F. 2d 981, 180 USPQ 580 (CCPA 1975). The examiner's proposed modification of Assar fails to establish a prima facie case of obviousness because, even if there were some motivation to develop the feature suggested by the examiner, the claim limitations are not taught or suggested by the reference. Rather, the proposed modification would maintain a separate counter of the number of erase cycles and then determine a total count of the number of erases based on the current counter value and the erase cycle counter. Contrary to this further complexity to Assar, the present invention provides an up-counter and then increases a maximum value when a majority to the blocks have counters near the maximum value.

In view of the above, applicant submits that claims 1-9, 11-13 and 15-17 are patentable over the teachings of Assar.

II. Rejection Under 35 USC §103(a) in view of Assar and Bruce

In tacit acknowledgment of any lack of foundation to the one-reference obviousness rejection, the examiner has offered an additional, two-reference obviousness rejection. Claim 1-3, 5-9 11-13, and 15-17 stand rejected under 35 U.S.C. 103(a) as unpatentable over Assar in view of U.S. Patent No. 6,000,006 to Bruce et al. ("Bruce").

The Bruce reference purports to improve upon the Assar methodology (compare col. 2, line 21 of Bruce to page 3, lines 25-32 of Assar). Assar periodically clears erase counters for respective blocks of memory, but does not maintain a count of the total number of erasures for a block over the lifetime of the memory. Bruce notes that the lack of this total number, as a result of the periodic clearing of the erase counters is undesirable (col. 2, lines 31(32)-33(34), and leads to uneven wear of the blocks over the long run (col. 2, lines 37-39). On the other hand, if Assar were to be modified to simply forego the clearing of erase counters would lead to inefficient page thrashing (col. 2, lines 39(40)-42(43)). In particular, although retention of the total erase counts advantageously affords longer-term wear leveling (col. 2, lines 36(37)-38(39)), Bruce nevertheless retains a periodically-cleared erase count which Bruce terms an "incremental-write count" (abstract, next-to-last sentence). The latter count is cleared at each wear-leveling operation for the block (col. 3, lines 6-8), whereas total-write count for the block is never cleared (abstract, next-to-next-to-last sentence). In Bruce, wear-leveling is performed only (col. 3, line 9: "must") when both (col. 3, line 8: "Both"; line 31(32): "both") a total-write threshold and an incremental-write threshold are exceeded by the respective incremental-write count and total-write count. In short, Bruce is not proposing to modify Assar. Bruce proposes to replace Assar.

Notably in this regard, Bruce operates in a manner fundamentally different than Assar. Bruce does not, for example, wear-level by copying data from one block to another as in Assar. Instead, Bruce performs wear-leveling by moving entries within a unified re-mapping table (col. 3, lines 11-13).

For at least all of the above reasons, the proposed combination of prior art references would not have rendered obvious the present invention. The instant two-reference obviousness rejection of claims 1-3, 5-9, 11-13 and 15-17 is accordingly invalid as to any of these claims.

III. Rejection Under 35 USC §103 (a) in view of Assar, Bruce and Marsters

Claim 14 stands rejected under 35 U.S.C. 103(a) as unpatentable over Assar in view of Bruce, or, alternatively, over Assar in view of Bruce and U.S. Patent No. 6,092,160 to Marsters.

Claim 14 depends from claim 1. Marsters is directed to block wear-leveling, but cannot make up for the deficiencies in Assar and Bruce. Accordingly, the proposed combination of references fails to render obvious the invention as recited in claim 14.

For at least all of the above reasons, the proposed combination of prior art references would not have rendered obvious the present invention.

IV. Rejection Under 35 USC §112, first and second paragraphs

Claims 15 and 17 stand rejected under 35 USC §112, first and second paragraphs.

With regard to claim 15, support for claim 15 is found in the specification (e.g., page 7, lines 25-29: "To avoid the block 22 being erased many more times . . . selecting a block whose counter has a lower value . . ."; page 6, line 25: "computer system"). As explained from page 7, line 23 to page 8, line 11, when the block 22 is determined to have an

unacceptable wear level, a block 23 of lower wear level is selected. Then, after data from block 22 is off-loaded to block 24, block 22 is erased and data from the block 23 is copied to block 22. Since block 22 now has data of lower wear level, block 22 avoids "being erased many more times." When the majority of blocks, for example, have wear levels that are unacceptable, i.e., their mutation counts exceed the limit value, the limit value is raised. Looking back at block 22 which has just received new data, block 22 is still subject to mutations, if, for example, the data in block 22 is program code and a user of the data on block 22 wants to make a revision to the program code (page 2, lines 15-26). This availability for mutations to block 22 exists even if the limit value has not since changed.

Each mutation for any given block occurs in a process that involves, for that block, a determination, and, depending on the result of the determination, either a mutation or a two-step process of (1) choosing and copying (2). This description of the process is clear from originally-filed claim 1, for example. In particular, determining is a first step. If the outcome of the determining is a particular result, then choosing and copying are executed. However, as a general proposition, the determining may occur a "number of times" (page 6, line 32: "number of times") before the choosing/copying are performed. If the limit value subsequently increases by much, the determining may again occur a "number of times" before the choosing/copying are performed. This "number of times" or iterative process is implicit from the above-described references to the specification and is inherent in the wording of claim 15.

Claim 15 recites, "determining whether . . . of the first block (22). . . is acceptable for executing the mutation, and if so, executing the mutation. . ., and otherwise choosing . . . and copying . . . wherein the blocks from said variety have an associated counter for counting the

number of mutations in the block concerned, . . . so that if said determining, said choosing and said copying are executed with respect to said first block . . . in a first iteration, said computer system is configured to, in the event of a second iteration with respect to said first block, again execute said determining even if said value of the counter of the first block (22) exceeded said limit value in said first iteration, said limit value not having since changed."

It would be clear to one of ordinary skill in the art that a first iteration and a second iteration are implicit in the cited portion of the present specification.

Claims 15 and 17 stand rejected under 35 U.S.C. 112, second paragraph, as indefinite for reciting a "first iteration" and a "second iteration."

As set forth in the previous section above, disclosure of these iterations is implicit in the cited portion of the specification.

> The examiner's focus during examination of claims for compliance with the requirement for definiteness of 35 U.S.C. 112, second paragraph is whether the claim meets the threshold requirements of clarity and precision, not whether more suitable language or modes of expression are available. When the examiner is satisfied that patentable subject matter is disclosed, and it is apparent to the examiner that the claims are directed to such patentable subject matter, he or she should allow claims which define the patentable subject matter with a reasonable degree of particularity and distinctness. Some latitude in the manner of expression and the aptness of terms should be permitted even though the claim language is not as precise as the examiner might desire. MPEP 2173.02.

In this regard, applicant submits that claim 15 is certainly worded with the "reasonable degree of particularity and distinctness" mandated in MPEP 2173.02.

Accordingly, the applicant does not believe that the instant grounds for rejecting claim 15 have merit.

IX. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Respectfully submitted,

Russell Gross
Registration No. 40,007

Date: December 7, 2004

By: Steve Cha
Attorney for Applicant
Registration No. 44,069

X. APPENDIX: THE CLAIMS ON APPEAL

1. A method of data management on a storage medium (10), the storage medium (10) comprising a variety of blocks (21) in which data can be stored, a first block (22) from said variety being selected to execute a mutation on, characterized by determining whether the wear level of the first block (22) is acceptable for executing the mutation, and if so, executing the mutation on the first block (22), and otherwise

- choosing from said variety a second block (23) with a lower wear level than the first block (22), and
- copying the data of the second block (23) to the first block (22),

wherein the blocks from said variety have an associated counter for counting the number of mutations in the block concerned, and a limit value is increased when a predetermined number, which is at least the majority, of the counters of the blocks from said variety exceed the limit value, said determining being based on said limit value and a value of the counter of the first block (22).

2. A method as claimed in claim 1, characterized in that when the value of the counter of the first block (22) is smaller than the limit value, the value of the counter is increased and the mutation is executed, and otherwise a block of which the counter has a lower value than the counter of the first block (22) is chosen as the second block (23).

3. A method as claimed in claim 2, characterized in that the lower value is the lowest value of the values of the counters of the blocks from said variety.

4. (Cancelled).

5. A method as claimed in claim 1, characterized in that the second block (23) is erased after the data of the second block (23) have been copied to the first block (22).

6. A method as claimed in claim 1, characterized in that the mutation comprises erasing the first block (22).

7. A system for data management on a storage medium (10), the storage medium (10) comprising a variety of blocks (21) in which data can be stored, the system being arranged for selecting a first block (22) from said variety to execute a mutation on, characterized by control means (26) for determining whether the wear level of the first block (22) is acceptable for executing the mutation, and if so, executing the mutation on the first block (22), and for otherwise

- choosing from said variety a second block (23) with a lower wear level than the first block (22), and
- copying the data of the second block (23) to the first block (22),

wherein the blocks from said variety have an associated counter for counting the number of mutations in the block concerned, and the control means (26) are arranged for increasing a limit value when a predetermined number, which is at least the majority, of the counters of the blocks from said variety exceed the limit value, said determining being based on said limit value and a value of the counter of the first block (22).

8. A system as claimed in claim 7, characterized in that the control means (26) are arranged for, when the value of the counter of the first block (22) is smaller than the limit value, increasing the value of the counter and executing the mutation, and for otherwise choosing a block of which the counter has a lower value than the counter of the first block (22) as the second block (23)

9. A system as claimed in claim 8, characterized in that the lower value is the lowest value of the values of the counters of the blocks from said variety.

10. (Cancelled).

11. A system as claimed in claim 8, characterized in that the system is arranged for initially constructing a table in which the value of the counters of the blocks are stated.

12. A system as claimed in claim 7, characterized in that the control means (26) are arranged for erasing the second block (23) after the data from the second block (23) have been copied to the first block (22).

13. A computer program product comprising a computer-readable medium and enabling a programmable device to function as a system as claimed in claim 7.

14. The method of claim 1, wherein said copying is preceded by the step of copying to another block (24) any stored data of said first block (22) that is not marked for erasure.

15. A method of data management on a storage medium (10), the storage medium (10) comprising a variety of blocks (21) in which data can be stored, a first block (22) from said variety being selected to execute a mutation on, characterized by determining whether the wear level of the first block (22) is acceptable for executing the mutation, and if so, executing the mutation on the first block (22), and otherwise

- choosing from said variety a second block (23) with a lower wear level than the first block (22), and
- copying the data of the second block (23) to the first block (22),

wherein the blocks from said variety have an associated counter for counting the number of mutations in the block concerned, and a limit value is increased when a predetermined number, which is at least the majority, of the counters of the blocks from said variety exceed the limit value, said determining being based on said limit value and a value of the counter of the first block (22), said method being configured for execution on a computer system so that if said determining, said choosing and said copying are executed with respect to said first block by said computer system in a first iteration, said computer system is configured to, in the event of a second iteration with respect to said first block, again execute said determining even if said value of the counter of the first block (22) exceeded said limit value in said first iteration, said limit value not having since changed.

16. The method of claim 1, wherein said predetermined number is equal to said majority.

17. The method of claim 15, wherein said processor copied data to said first block in said first iteration as a result of determining that said value of the counter of the first block exceeded said limit value.

18. (Canceled).